

Notice of References Cited	Application/Control No. 10/679,266		Applicant(s)/Patent Under Reexamination MANTRI, PRASAD	
	Examiner John P. Trimmings		Art Unit 2138	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,674,090	06-1987	Chen et al.	714/736
*	B	US-6,657,878	12-2003	Lien et al.	365/49
*	C	US-4,680,760	07-1987	Giles et al.	714/718
*	D	US-2005/0050408	03-2005	Kaginele, Sathya P.	714/718
*	E	US-5,107,501	04-1992	Zorian, Yervant	714/720
*	F	US-6,496,950	12-2002	Zhao et al.	714/718
	G	US-			
	H	US-			
	T	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wright et al., "Transistor-Level Fault Analysis and Test Algorithm Development for Ternary Dynamic Content Addressable Memories", IEEE Test Conference 2003, Vol. 1, 10-02-2003, pp 39-47.
	V	Patel et al., "Circuits for Low Power Bus Traffic Encoding", Semester Project, located at: http://www.cs.berkeley.edu/~yatish/ee241/ee241_yatish_yurym_projreport.pdf , accessed on 2/13/2006 using Google Search.
	W	Zhao et al., "Testing SRAM-Based Content Addressable Memories", IEEE Transactions on Computers, Vol. 49, No. 10, October 2000.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.